CLAIMS

1. A method of fabricating a semiconductor device, the method comprising:

forming a gate dielectric made of high dielectric permittivity material;

depositing, directly on the gate dielectric, a $Si_{1-x}Ge_x$ first layer, where $0.5 < x \leq 1$, at a temperature substantially below the temperature at which the poly-Si is deposited by thermal chemical vapor deposition (CVD); and

depositing a $Si_{1-y}Ge_y$ second layer, where $0 \leq y \leq 1$, on top of the $Si_{1-x}Ge_x$ first layer.

2. The method of claim 1, wherein the $Si_{1-x}Ge_x$ first layer is deposited by thermal CVD.

3. The method of claim 1, wherein at least one of the $Si_{1-x}Ge_x$ first layer and the $Si_{1-y}Ge_y$ second layer is predominantly Ge.

4. The method of claim 1, wherein $0.7 \leq x \leq 1$.

5. The method of claim 1, wherein x=1.

6. The method of claim 1, wherein $0.7 \leq x \leq 1$ and $0.7 \leq y \leq 1$.

7. The method of claim 6, wherein x=y=1.

8. The method of claim 1, wherein the $Si_{1-x}Ge_x$ first layer is doped in situ so that doping in is in a presence of dopants in a gas mixture used to deposit the $Si_{1-x}Ge_x$ first layer.

9. The method of claim 1, wherein the $Si_{1-y}Ge_y$ second layer is doped in situ so that doping in is in a presence of dopants in a gas mixture used to deposit the $Si_{1-y}Ge_y$ second layer.

10. The method of claim 1, further comprising:

diffusion annealing so that at least one of Ge and Si diffuse betweenthe $Si_{1-x}Ge_x$ first layer iand the $Si_{1-y}Ge_y$ second layer.

11. The method of claim 1, wherein the gate dielectric is selected in a group of metal oxides consisting of HfO_2, ZrO_2, HfSiO and ZrSiO.

12. A semiconductor device comprising:

a substrate;

a gate dielectric deposited on the substrate, wherein the gate dielectric is made of high dielectric permittivity material; and

a gate formed on top of a $Si_{1-x}Ge_x$ first layer comprising:

a $Si_{1-x}Ge_x$ first layer formed directly on the gate dielectric, where $0.5 < x \leq 1$; and,

a $Si_{1-y}Ge_y$ second layer, formed on top of the $Si_{1-x}Ge_x$ first layer where $0 \leq y \leq 1$.

13. The semiconductor device of claim 12, wherein at least one of the $Si_{1-x}Ge_x$ first layer and the $Si_{1-y}Ge_y$ second layer is predominantly Ge.

14. The semiconductor device of claim 12, wherein the gate further comprises a layer for limiting the diffusion of at least one of Ge and Si between the $Si_{1-y}Ge_y$ second layer and the $Si_{1-x}Ge_x$ first layer.

15. The semiconductor device of claim 12, wherein the gate dielectric is selected in a group of metal oxides consisting of HfO_2, ZrO_2, HfSiO and ZrSiO.

16. The semiconductor device of claim 12, wherein x=1.

17. The semiconductor device of claim 12, wherein x=y=1.

18. The semiconductor device of claim 12, wherein an interface between the gate dielectric and the gate is predominantly made of Si.